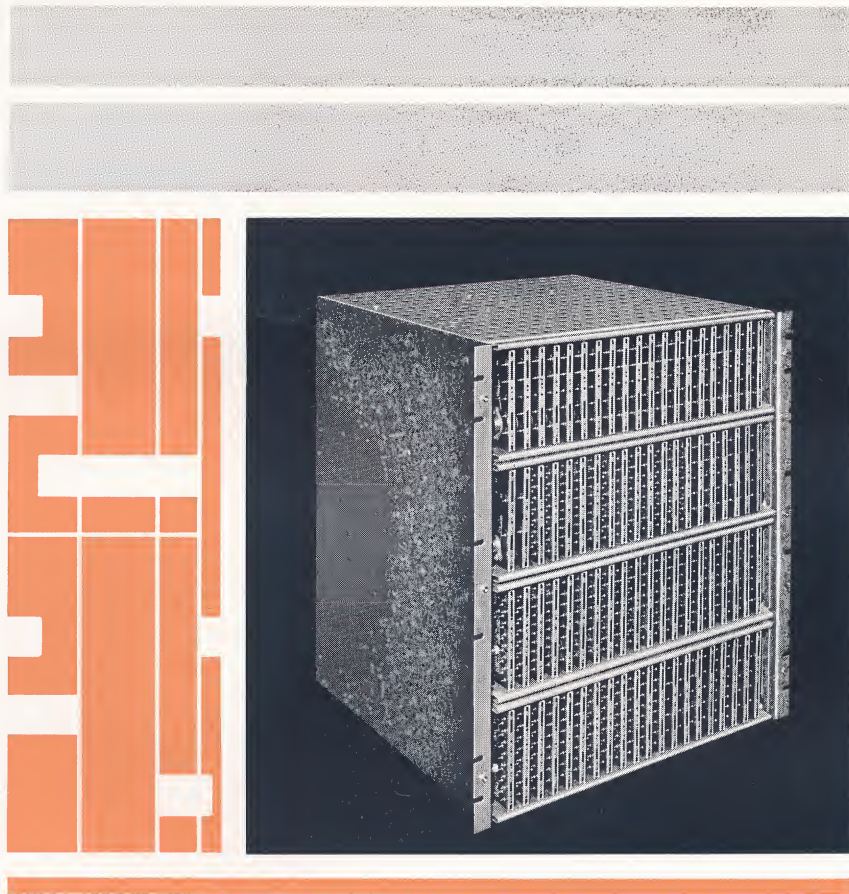




applications guide to magnetic core --

MEMORY SYSTEMS

SERIES:	M	L	K	J	I	H	G	F	S	R	U	T
FULL CYCLE— μ sec.	10		6		5		4		3		2	
HALF CYCLE— μ sec.	10	5		3		2.5		2		1.6		1.1

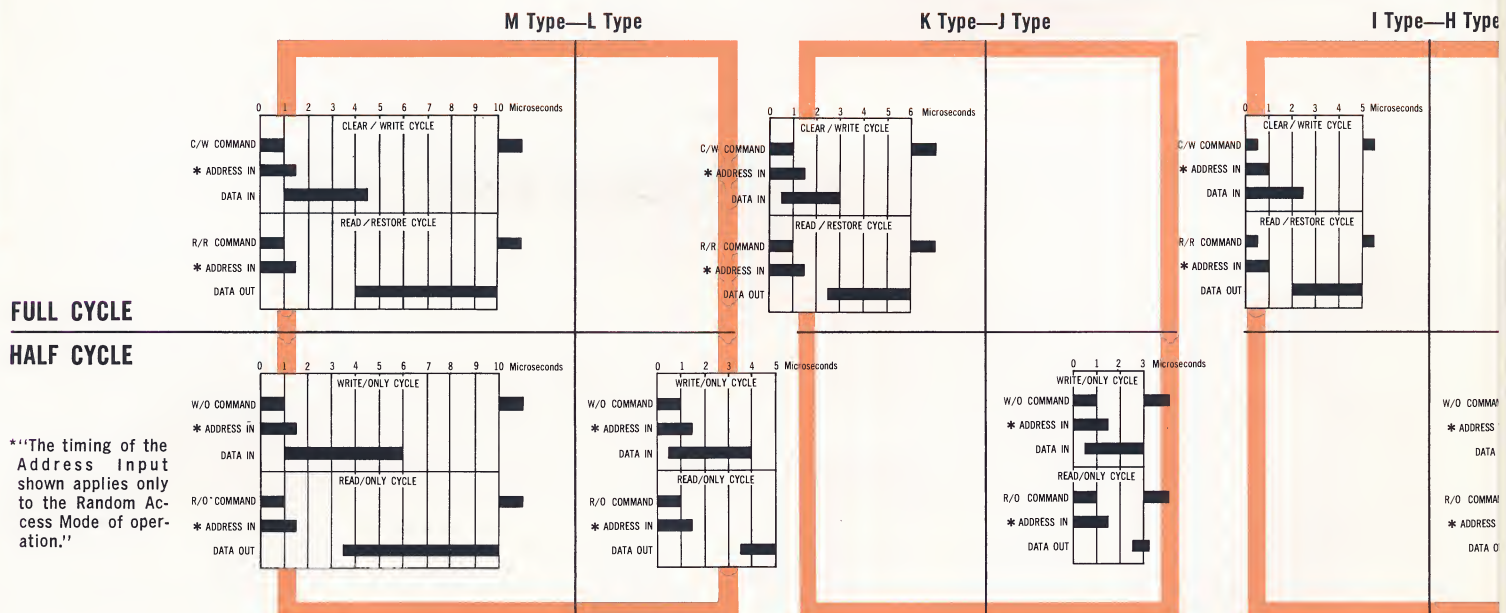
SERIES Specification . . .

SERIES	M		L		K	J		I	
CYCLE TIME	10 μ sec. (Full Cycle)	10 μ sec. (Half Cycle)	5 μ sec. (Half Cycle)		6 μ sec. (Full Cycle)	3 μ sec. (Half Cycle)		5 μ sec. (Full Cycle)	2 μ sec. (Half Cycle)
DATA ACCESS TIME	3.5 μ sec.	3.5 μ sec.	3.5 μ sec.		2.5 μ sec.	2.5 μ sec.		2 μ sec.	1 μ sec.
CAPACITY . . . (Any bit length desired)	AS REQUIRED				AS REQUIRED			AS REQUIRED	
ACCESS MODES	Random Access Sequential Non-Interlaced Sequential Interlaced Random/Sequential Non-Interlaced Random/Sequential Interlaced				Random Access Sequential Non-Interlaced Sequential Interlaced Random/Sequential Non-Interlaced Random/Sequential Interlaced			Random Access Sequential Non-Interlaced Sequential Interlaced Random/Sequential Non-Interlaced Random/Sequential Interlaced	
OPERATIONS†	Clear/Write Read/Restore	W/O R/O	W/O R/O		Clear/Write Read/Restore	W/O R/O		Clear/Write Read/Restore	W/O R/O
COMMAND SIGNALS: { Amplitude Rise Time Duration Fall Time	6 volts (negative going) $\leq 0.3\mu$ sec. 1.0 μ sec. (40% Duty Factor) $\leq 0.3\mu$ sec.				6 volts (negative going) $\leq 0.3\mu$ sec. 1.0 μ sec. (40% Duty Factor) $\leq 0.3\mu$ sec.			6 volts (negative going) $\leq 0.2\mu$ sec. 0.5 μ sec. (40% Duty Factor) $\leq 0.2\mu$ sec.	
ADDRESS INPUTS DATA INPUTS DATA OUTPUTS	Binary "1": -6 volts Binary "0": 0 volts				Binary "1": -6 volts Binary "0": 0 volts			Binary "1": -6 volts Binary "0": 0 volts	
ENVIRONMENT: Operating Temperature†† Relative Humidity Storage Temperature	0°C to 50°C Up to 95% -55°C to +65°C				15°C to 40°C Up to 95% -55°C to +65°C			15°C to 40°C Up to 95% -55°C to +65°C	
POWER REQUIREMENTS	117 volts A.C. $\pm 10\%$ 60 CPS ± 3 cycles, single phase				117 volts A.C. $\pm 10\%$ 60 CPS ± 3 cycles, single phase			117 volts A.C. $\pm 10\%$ 60 CPS ± 3 cycles, single phase	
MOUNTING	Std. 19" & 24" Relay Racks				Std. 19" & 24" Relay Racks			Std. 19" & 24" Relay Racks	
FINISH	Federal Standard No. 595 Color No. 25193, Blue, Wrinkle				Federal Standard No. 595 Color No. 25193, Blue, Wrinkle			Federal Standard No. 595 Color No. 25193, Blue, Wrinkle	

†Refer to definitions on Page 2

††Forced draft required

Timing Charts



Optional Features . . .

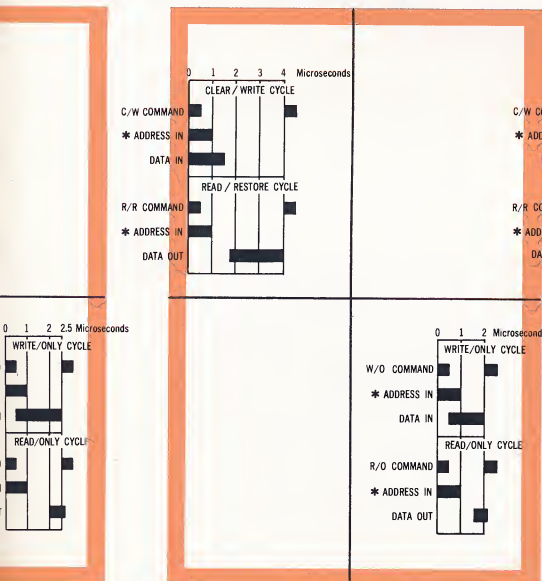
■ INDICATOR LIGHTS ■ REMOTE POWER SUPPLY ■ BUILT IN TEST AND PARITY MODES ■ SPARE CARDS AND COMPONENTS KIT ■ ADDRESS



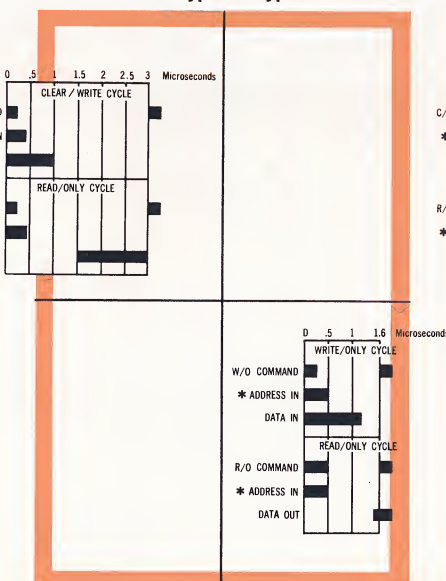
H		G	F		S	R		U	T
4 μ sec. (Full Cycle)		4 μ sec. (Full Cycle)	2 μ sec. (Half Cycle)		3 μ sec. (Full Cycle)	1.6 μ sec. (Half Cycle)		2 μ sec. (Full Cycle)	1.1 μ sec. (Half Cycle)
4 μ sec.		1.75 μ sec.	1.75 μ sec.		1.5 μ sec.	1.5 μ sec.		1 μ sec.	1 μ sec.
		AS REQUIRED			AS REQUIRED			AS REQUIRED	
Interlaced aced		Random Access Sequential Non-Interlaced Sequential Interlaced Random/Sequential Non-Interlaced Random/Sequential Interlaced			Random Access Sequential Non-Interlaced Sequential Interlaced Random/Sequential Non-Interlaced Random/Sequential Interlaced			Random Access Sequential Non-Interlaced Sequential Interlaced Random/Sequential Non-Interlaced Random/Sequential Interlaced	
W/O R/O		Clear/Write Read/Restore	W/O R/O		Clear/Write Read/Restore	W/O R/O		Clear/Write Read/Restore	W/O R/O
ing) actor)		6 volts (negative going) $\leq 0.2 \mu$ sec. 0.5 μ sec. (40% Duty Factor) $\leq 0.2 \mu$ sec.			6 volts (negative going) $\leq 50N$ sec. 0.3 μ sec. (40% Duty Factor) $\leq 50N$ sec.			6 volts (negative going) $\leq 50N$ sec. 0.3 μ sec. (40% Duty Factor) $\leq 50N$ sec.	
ts ts		Binary "1": -6 volts Binary "0": 0 volts			Binary "1": -6 volts Binary "0": 0 volts			Binary "1": -6 volts Binary "0": 0 volts	
C		15°C to 40°C Up to 95% -55°C to +65°C			15°C to 35°C Up to 95% -55°C to +65°C			15°C to 35°C Up to 95% -55°C to +65°C	
% phase		117 volts A.C. $\pm 10\%$ 60 CPS ± 3 cycles, single phase			117 volts A.C. $\pm 10\%$ 60 CPS ± 3 cycles, single phase			117 volts A.C. $\pm 10\%$ 60 CPS ± 3 cycles, single phase	
acks		Std. 19" & 24" Relay Racks			Std. 19" & 24" Relay Racks			Std. 19" & 24" Relay Racks	
595 Wrinkle		Federal Standard No. 595 Color No. 25193, Blue, Wrinkle			Federal Standard No. 595 Color No. 25193, Blue, Wrinkle			Federal Standard No. 595 Color No. 25193, Blue, Wrinkle	

ts . . . The timing bars indicate steady state conditions

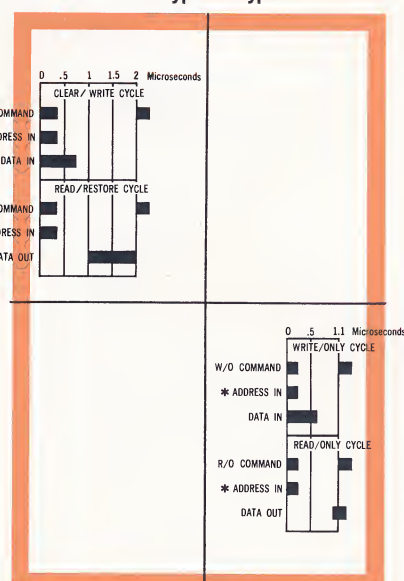
G Type—F Type



S Type—R Type



U Type—T Type



Standard **MEMORY SYSTEMS** Assemblies . . .

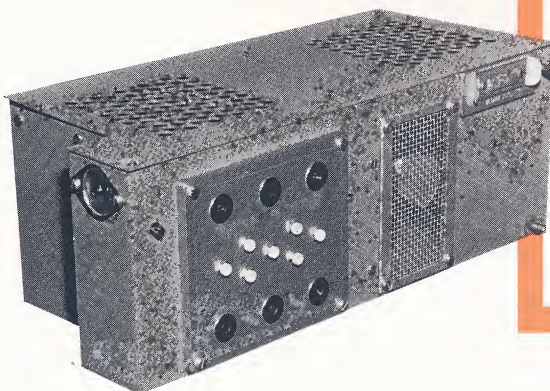
Power Supplies



"Rack Mounted Model #2013."



"Double Deck Rear Mounted Model #2012."



"Single Deck Rear Mounted Model #2011."

GENERAL SPECIFICATIONS:

Power Requirement—Units operate from an input voltage of $117 \pm 10\%$ VAC, 60 ± 3 cycles, single phase.

D.C. Output Voltage—Each D.C. output voltage can be varied over a range of $\pm 15\%$ by means of controls located on the front panel.

Dynamic Load Regulation—Less than 1.8% for a load change from zero to a maximum current rating.

Dynamic Line Regulation—Less than 1.8% for line fluctuations at $117 \pm 10\%$ VAC.

Ripple Voltage—Output voltage less than 0.4% r m s (under worse line and load conditions).

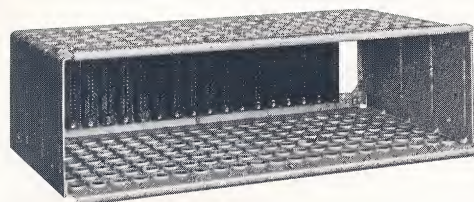
Stability—Output voltage variation for a period of eight hours is less than 0.5%. Each module is checked for drift over an eight hour period.

Response Time—Less than 50 microseconds for a load step change of from 0 to 100% of full load.

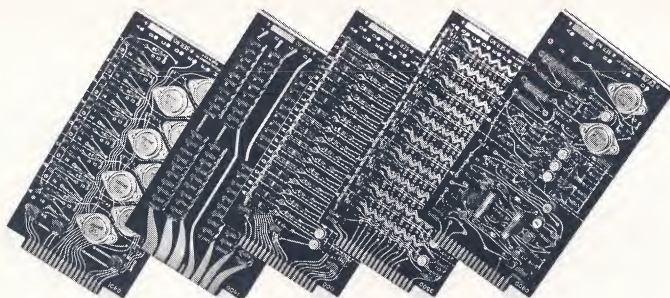
Overload Protection (Electrical)—Each voltage supply is separately fused. Current overload of any one voltage supply will blow a fuse, removing primary power. Blown fuse is indicated by a light on the front panel.

Thermal—A thermostat in each power supply plenum chamber opens at 56°C , removing primary power. Thermal overload is indicated by a light on the front panel.

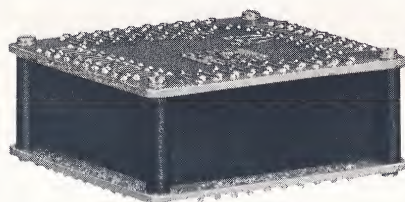
Air Cooling—Each power supply plenum chamber is equipped with a blower motor to provide positive displacement of warm air. Screened vent(s) on the front panel and an opening on one side of each plenum chamber provides for cool air intake and warm air discharge.

**MS-1****Card Cage**

- unitized construction in std. 19" & 24" relay rack sizes
- vent holes spaced for optimum ventilation
- cards spaced within cage for optimum heat distribution
- solderless card edge connectors
- plastic wiring ducts for harnessing
- card locations numbered on cage

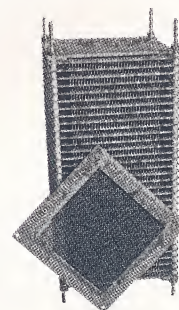
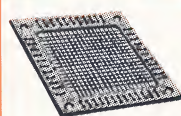
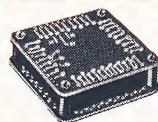
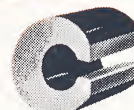
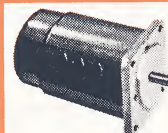
**Printed Circuit Cards**

- readily accessible test points provided for each circuit on card
- finger grip handle with title insert giving functional description of card
- silk screened component callouts
- gold plated copper wiring with plated through-holes
- gold plated copper contacts

**Memory Stack**

- compact miniaturized **MICROSTACK®** or printed circuit stack
- printed circuit terminals
- meets shock and vibration requirements of Mil. T-4807 (1A), Mil. Std.—202 B (202A + 204A)

All system components both manufactured and purchased receive extensive incoming inspection tests prior to release for system fabrication. Initial system test begins with individual wave form inspection tests on individual cards in the rack position. This continues until the entire unit is operational. Shock tests are conducted while the unit is connected to an IGC memory system exerciser which compares input-stored data to the read-out data. After error-free operation is obtained during the shock test, the unit is then subjected to the highest specified operating temperature. When thermal equilibrium is reached, the unit is tested for error-free operation under all specified voltage margins with minimum input signal levels. Voltage margins are $\pm 10\%$ on all power supply voltages with the exception of the plus 22V supply. This supply is only allowed an excursion of $\pm 5\%$ since it determines the drive current through the core array. The input line voltage is varied $\pm 10\%$. The unit is then subjected to the lowest specified temperature, and the above test is again repeated. During all the above tests, the unit is subjected to data patterns as follows: all binary ONES, all binary ZEROS, worst pattern, and worst pattern complement and must operate error free for eight hours at each temperature extreme.

**INDIANA GENERAL CORPORATION****ELECTRONICS DIVISION • Keasbey, New Jersey • Phone VALley 6-5100****MEMORY PRODUCTS, FERRITES AND STEATITE INSULATORS****MEMORY
PLANES****MEMORY
STACKS****FERRITE
INDUCTORS****PERMANENT
MAGNETS****MINIATURE
MOTORS**